Amendments to the Specification

Please replace the paragraph beginning at page 2, line 20, with the following rewritten paragraph.

--As shown in Fig. 1, the system 10 includes a core unit, indicated by a dashed enclosure 12, for performing various operations as discussed hereinbelow in connection with Figs. 1-4 ~~Figs. 1-5~~. The core unit 12 includes: (a) a program sequencer unit 14; (b) a resource stall unit 16; (c) an address generation unit ("AGU"), indicated by a dashed enclosure 18; and (d) a data arithmetic logic unit ("DALU"), indicated by a dashed enclosure 20. The AGU includes arithmetic address units ("AAUs") 22, a bit mask unit ("BMU") 24, and an address generator register file 26. The DALU includes arithmetic logic units ("ALUs") 28 and a DALU register file 30. The program sequencer unit 14, resource stall unit 16, AGU 18 (including its various units and files), and DALU 20 (including its various units and files) are interconnected as shown in Fig. 1.--

Please replace the paragraph beginning at page 7, line 7, with the following rewritten paragraph.

--The multi-stage pipeline of the system 10 includes multiple execution stages. For example, in the illustrative embodiment as described in Table 2, the pipeline includes a first execution stage (E-stage) and a second execution stage (M-stage). In an alternative embodiment, the pipeline includes first and second execution stages, plus at least one additional execution stage. In such an alternative embodiment, the respective operations of the multiple execution stages are suitably established, according to the various objectives of the system 10, so that one or more of the E-stage or M-stage operations (which are described in Table 2 and elsewhere hereinbelow in connection with Figs. 2-4 ~~Figs. 2-5~~) is/are performed instead (or additionally) by a suitable one or more of the multiple execution stages.--

Please replace the paragraph beginning at page 9, line 2, with the following rewritten paragraph.

--Fig. 2 is a block diagram of the program sequencer unit 14. As shown in Fig. 2, the program sequencer unit 14 includes an instruction fetch buffer 50, a sequencer logic 52, a program address control logic 54, an address buffer 56, and a current address register 58. Such elements of the program sequencer unit 14 perform various operations as discussed hereinbelow in connection with Figs. 2-4 ~~Figs. 2-5~~.--